Claims

1. A method of forming at least one, preferably a plurality of, dielectrically insulating isolation trenches (2), in particular as an insulation trench, for the (dielectric) isolation of regions of different potential, in particular, of device structures (B) formed above an SOI wafer (A1, A2) including an active semiconductor layer, by allowing at least one void (11) formed by filling an insulating material in said at least one isolation trench, thereby forming a hermitically tight seal (14) of the at least one void with respect to the semiconductor wafer surface,
the method comprising a sequence of CMOS process steps after forming the at least one trench (2),
the sequence comprising performing a first fill step in the form of a controlled deposition, preferably a SiO_2 deposition (7; 7', 7''), adapted to trench geometry, in particular based on a CVD process, thereby forming oxide layers, in particular SiO_2 layers (7', 7'') at trench walls, said oxide layers having an increasing thickness towards to upper trench edges (2a', 2a'') and forming a first bottleneck (8).

2. A method of forming at least one, preferably a plurality of, dielectrically insulating isolation trenches (2), preferably according to claim 1, comprising (subsequently) anisotropically RIE etching the oxide layer (7) in a first step until the oxide layers, in particular the SiO_2 layers are removed from the wafer surface and subsequently continuing the etch process in a second step for removing the oxide layer in an upper trench portion to a defined depth (a7, a8) for defining of a later sealing portion of the void (11) or for displacing downwardly the first bottleneck to a further bottleneck (8a).

3. A method of forming at least one, preferably a plurality of, dielectrically insulating isolation trenches (2), preferably according to claims 1 or 2, comprising a (subsequent) second oxide deposition, in particular an SiO_2 deposition, by a low pressure CVD process, thereby again preferably depositing an oxide near a step formed previously and/or at the displaced bottleneck (8a), resulting in sealing (14) a void (11) located below, said deposition process being stopped when the sealed portion (14) of the oxide layer above said void (11) is grown above a wafer level (3b, 4b) of the semiconductor layer (1).

4. The method of claims 1 or 3 and 2, wherein after sealing said trench (filling) the wafer surface is planarized and a technological process sequence is continued.

5. The method of claim 2, wherein the back etching of the first trench filling (7) in the area outside said trench stops on a polysilicon layer (6), which has previously been formed on a silicon dioxide layer (5) or on a multi insulator layer.

6. The method of claims 1 or 3, wherein the same process technique is used during the first and the second SiO_2 depositions.

7. The method of claims 1 or 3, wherein the different process techniques are used during the first and the second SiO_2 depositions, in particular in view of an efficient and a less efficient isotropic insulator deposition.

8. The method of claim 1, applied to an SOI wafer, said SOI wafer comprising micro electronic mechanic systems (MEMS) in a semiconductor layer (1) formed on the oxide layer.

9. The method of claim 1, wherein the at least one trench has a high aspect ratio, preferably higher than 15:1.

10. The method of claims 1 or 3, wherein the formed sealed at least one void (11) is located below the level of the surface (3b, 4b) of the active semiconductor layer (19).

11. The method of claim 1, wherein a surface of the sealed trench is planarized.

12. open

13. A processed SOI wafer comprising at least one insulation trench (2) having a sealed void (11), an upper end (12) of said void ending below a surface (3b, 4b) of an active semiconductor layer (1) of the SOI wafer, said SOI wafer formed or formable according to any of claims 1 to 12.

14. The SOI wafer according to the preceding claim, wherein a notch tip (13) extending downwardly and located above said sealed trench (2, 9, 10)

terminates above a (horizontal) level of the surface (3b, 4b) of the active semiconductor layer with a vertical distance (c).

15. A method for filling isolation trenches (2) having a high aspect ratio for dielectrically isolating regions of different potentials of device structures formed on an SOI wafer by forming, based on the insulator filling of the respective trench, a void (11) having a hermetically tight sealing below a level of the semiconductor wafer surface (4b, 3a, 3b), and by planarizing subsequent to the filling of the trench having the maintained void (11) and by performing a sequence of CMOS process steps after forming said trench:

- forming SiO_2 layers (7; 7'', 7') by a CVD process, said SiO_2 layers having a thickness increasing towards the upper trench edges,
- completely removing SiO_2 portions at the upper trench portion to a defined depth so as to determine a later sealing point (12) of the void (11), by a substantially anisotropic etch process, thereby creating a step at a narrowest portion (8a) in the trench (2, 9),
- sealing a respective void (11) and filling the respect trench by depositing a second SiO_2 layer (10) by a low pressure CVD process such that a tip of a notch (13) of the formed second oxide layer is positioned above (c) the level of the semiconductor wafer surface (4b, 3a, 3b).

16. The method of claim 15, wherein back etching the first trench filling – as the complete removal of the SiO_2 layer portions in the upper trench portion to the defined depth – is terminates in the region outside said trench at a polysilicon layer formed on at least one silicon dioxide layer.

17. The method of claim 15, wherein the same process technique is used in the first and second SiO_2 depositions.

18. The method of claim 15, wherein different process techniques are used in the first and second SiO_2 depositions.

19. The method of claim 15, used for SOI wafers comprising microelectronic mechanic systems (MEMS) in the semiconductor layer formed above the oxide layer.

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